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|--|-----|----|--------------|------------------------|--------------|--|
| | | | 01.001.05 | Application Number | 10/064,215 | |
| | | | CLOSURE | Filing Date | 08/21/2002 | |
| STATEMENT BY APPLICANT | | | | First Named Inventor | Jyh-Fong Lin | |
| | | | | Group Art Unit | 2839 | |
| (use es many sheets as necessary) | | | s necessary) | Examiner Name | | |
| Sheet | . 1 | of | 1 | Attorney Docket Number | VIAP0029USA | |

| OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS | | | | | | | | |
|---|--------------|--|---------|--|--|--|--|--|
| Examiner Initials | Cite No.1 | Include name of the surnor (in CAPITAL LETTERS), tide of the article (when appropriate), tide of the fram (book, magazine, journal, serial, sympostum, catalog, etc.), date, page(s), volume-tasue number(s), number(s), number(s) and/or country where numbers. | Ţ | | | | | |
| N.E. | 1 | WANG RUC-PENG, L I SHU-GUANG, ZHENG ZENG-YU; A Clock and Data Recovery Circuit for 10-Mb/s and 100-Mb/s Ethernet; Microelectronics; Aug. 2002; page 308 - page 311; Vol. 32 No. 4 | ŀ | | | | | |
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¹ Applicant's unique custon designation number (optional). 2 Applicant is to place a check mark hore it English tenguage Translation is situched.

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